

Siloti™ Visibility Automation System



VERIFICATION ENHANCEMENT SOLUTIONS

The Siloti™ Visibility Automation System transforms your verification methodology by eliminating the overhead associated with recording data for all the signals in a design. Unique automation technology in the Siloti system provides you full visibility of internal signals for complex IC and system-on-chip (SoC) designs by:

- Identifying the minimal set of signals that must be recorded,
- Generating “on-demand” the rest of the signal data, and
- Correlating gate-level results to the register transfer level (RTL) source code.

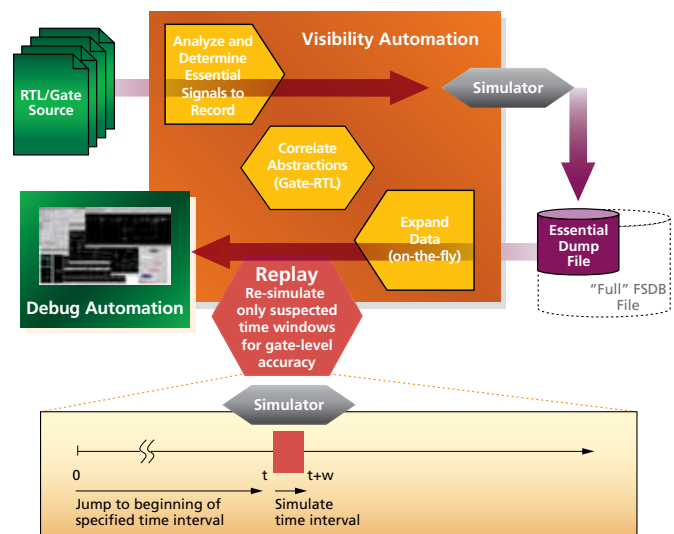
The Siloti system is used during full-chip simulation allowing you to:

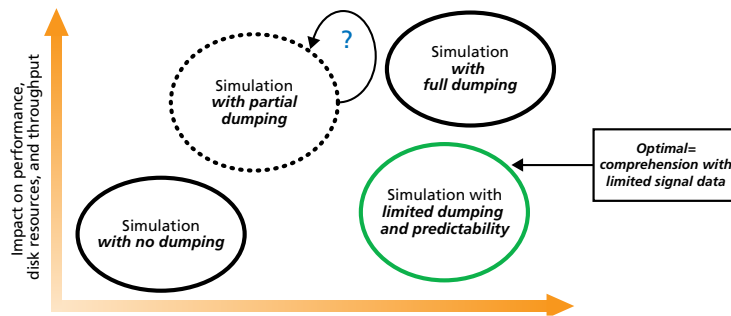
- Achieve full visibility into the functional operation of designs with minimal impact on verification performance;
- Analyze and debug gate-level verification results on the RTL design; and thus
- Reduce overall verification time and cost.

Improve Verification Throughput and Predictability

Powerful, breakthrough visibility automation technologies accelerate your process for understanding and correcting the causes of incorrect design behavior by:

- Deriving a minimum set of “essential” signals to be recorded during verification;
- Analyzing the limited set of recorded signal data and automatically regenerating missing information; and
- Correlating signal data associated with low-level chip representations with corresponding RTL descriptions.





Inadequate Visibility Hampers Verification

Observing enough signals to analyze and isolate the root causes of problems found during verification of large designs is increasingly difficult, expensive, and time-consuming due to:

- The massive amounts of data produced;
- Performance degradation due to recording of signal data at verification run time;
- Limitations on the amount and type of signal data accessible using some hardware-based verification; and
- Difficulties in interpreting signal data recorded when simulating unfamiliar low-level design representations.

Visibility Automation Technologies

The Visibility Automation technology in the Siloti system combines Visibility Analysis techniques and a Data Expansion engine to reduce the impact of observation on the performance of your critical design and verification resources.

Visibility Analysis Engine

- Analyzes RTL and netlist representations to determine the minimum set of essential signals required for full visibility when used with Siloti data expansion and
- Provides the flexibility needed to target your entire design or only those blocks and signals of interest.

Data Expansion Engine

- Automatically computes signal data for the signals you did not record based on the recorded essential signal data and design knowledge provided by RTL or netlist and
- Optimizes the data regeneration process by computing "on-demand" only those values you require.

In addition to these core capabilities, the optional Siloti Abstraction Correlation and Replay modules make visibility and verification of your gate-level verification results more efficient.

Abstraction Correlation Module

- Automatically maps gate-level verification results to RTL design descriptions and
- Interoperates seamlessly with the data expansion engine enabling you to analyze and debug with full visibility on the RTL design.

Replay Module

- Operates on recorded essential signal data;
- Enables incremental, timing-accurate simulations for specified time windows, eliminating the need for you to re-run full timing simulation when an error is detected; and
- Provides full visibility for all signals in specified time windows, enabling you to quickly analyze and debug timing errors.

Optimize Verification and Validation Methodologies

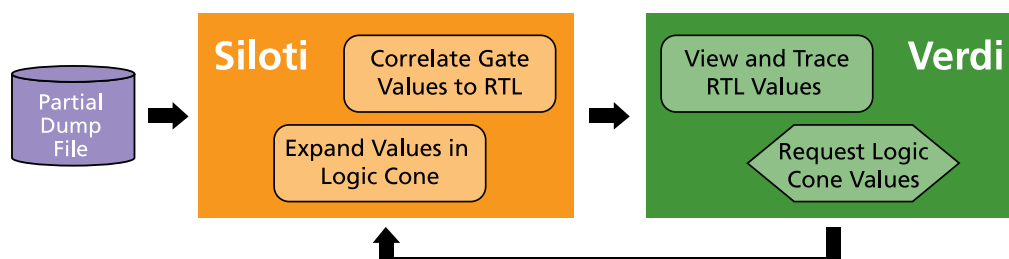
The capabilities of the Siloti Visibility Automation System dramatically improve full-chip simulation, emulation, first-silicon prototype and silicon validation methodologies. It speeds comprehension of design operation when errors are discovered and enables better utilization of your verification resources by:

- Minimizing the set of signals recorded during simulation, thereby improving run time performance and reducing dump file size while retaining full visibility;
- Eliminating multiple simulation iterations typically required to isolate and fix problems;
- Reducing the data that must be captured during slow, timing-accurate gate-level simulations;
- Minimizing the set of signals probed during emulation or prototype operation, thus improving verification performance while retaining full visibility; and
- Correlating gate-level verification results back to RTL source for easy understanding and debug of design behavior.

Accelerate Debug and Analysis — Seamless Integration Between Siloti and Verdi

The Siloti visibility automation system is fully integrated with the market-leading Verdi™ Automated Debug System so that you can leverage the benefits of an “essential” signal dump to retain full visibility for the most efficient gate or RTL debug. You can move seamlessly between the Siloti system and the Verdi system regardless of how many or which signals in your design you record. The Verdi system will detect if the information being received is coming from the Siloti essential signal FSDB and will automatically invoke the data expansion engine to quickly view the signal details for debug. There is no need to switch back and forth between systems. You can take advantage of the powerful visualization and automation capabilities in the Verdi system to:

- Extract, isolate and display relevant logic in flexible and powerful design views;
- Automate behavior tracing with unique behavior analysis technology; and
- Reveal the operation and interaction between the design, assertions and testbench.



The Siloti Visibility Automation environment provides the Verdi Automated Debug System with requested signal value data “on-demand”, optimizing performance and compute memory resources.

The Siloti Visibility Automation System Eliminates Simulation Overhead

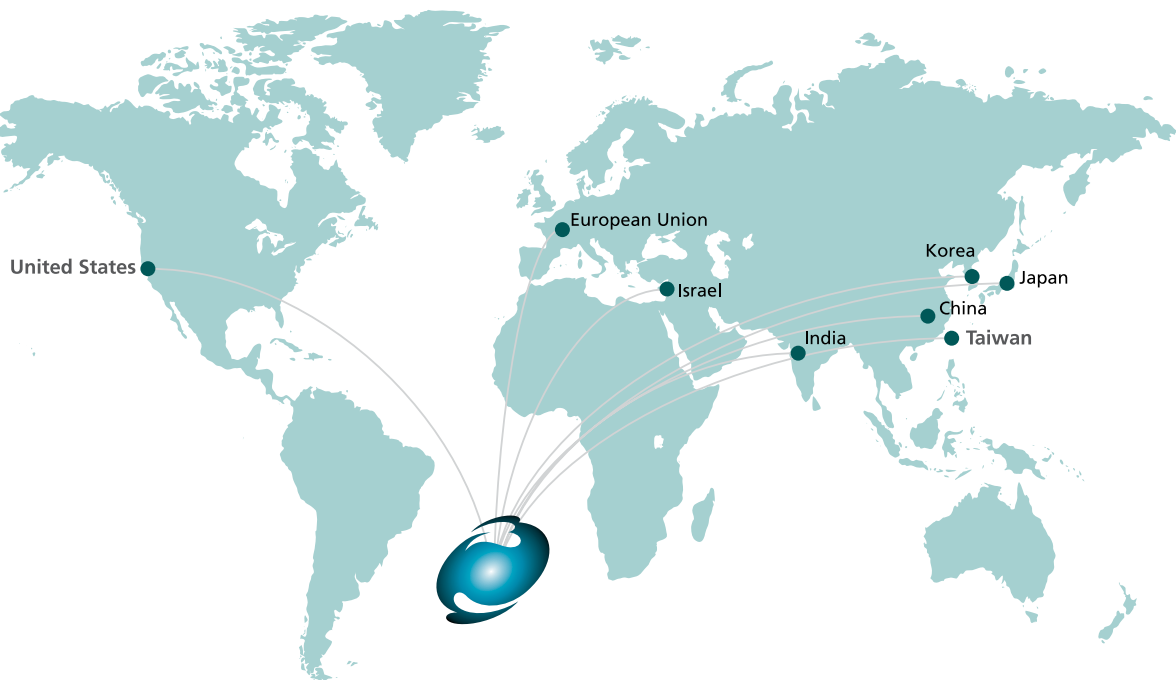
SpringSoft’s Verification Enhancement solutions include the Siloti Visibility Automation system to solve the costly problem of decreased signal visibility during full-chip simulation, emulation, first-silicon prototyping and system validation. You can immediately realize the benefits of greater design comprehension, more predictable verification and validation cycles, and faster debug of complex ICs and SoCs.

Siloti™ Visibility Automation System



VERIFICATION ENHANCEMENT SOLUTIONS

SpringSoft Offices



United States

SpringSoft USA
(Headquarters)
2025 Gateway Place
Suite 400
San Jose, CA 95110
Tel: (408) 467-7888
Fax: (408) 467-7889
www.springsoft.com

Taiwan

SpringSoft Taiwan
(Headquarters)
No. 25, Industry East Road IV,
Science-Based Industrial Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: +886 (3) 579-4567
Fax: +886 (3) 579-9000
www.springsoft.com/ch/

Europe & Israel

SpringSoft Inc. Europe Office
SpringSoft Design Automation Ltd
Synegis House
21 Crockhamwell Road
Woodley, Reading RG5 3LE UK
Phone/Fax: +44(0)11890 76389
www.springsoft.com

South East Asia

Waiz Pte Ltd
23 Springleaf View
Singapore 787928
Tel: +65-64515217
Fax: +65-64515217
www.waiz.info/

Japan

SpringSoft K.K., Inc.
KAKIYA Bldg. 6F 2-7-17
Shin-Yokohama, Kohoku-ku,
Yokohama 222-0033 Japan
Tel: +81 (45) 470-8890
Fax: +81 (45) 470-8891
www.springsoft.com/jp/

Korea

Kitec Design Technology Co., Ltd,
SinDo Bldg 2FL, 10,
Garak-Dong, Songpa-Gu,
Seoul, Korea, 138-800
Tel: +82 (2) 2140-5500
Fax: +82 (2) 2140-5555
www.ktdesign.co.kr/

China / Hong Kong

SpringSoft Co., Ltd.
(Shanghai)
Room A, 5FL, 398 Tianlin Rd.,
Shanghai, 200233 China
Tel: +86-21-54902090
Fax: +86-21-54902093
www.springsoft.com/sch/

India

CMR Design Automation P. Ltd,
Bangalore
3516, 14th 'A' Main, Indiranagar,
HAL IIInd stage,
Bangalore, PIN:- 560008 India
Tel: +91-80-5276866/5261274
Fax: +91-80-5279741
www.cmrda.com/

CMR Design Automation P. Ltd, Delhi

E-534, Greater Kailash - II,
New Delhi, PIN:- 110048 India
Tel: +91-11-6477085/8637128
Fax: +91-11-6213498