

Verdi™ Power-Aware Debug Module



VERIFICATION ENHANCEMENT SOLUTIONS

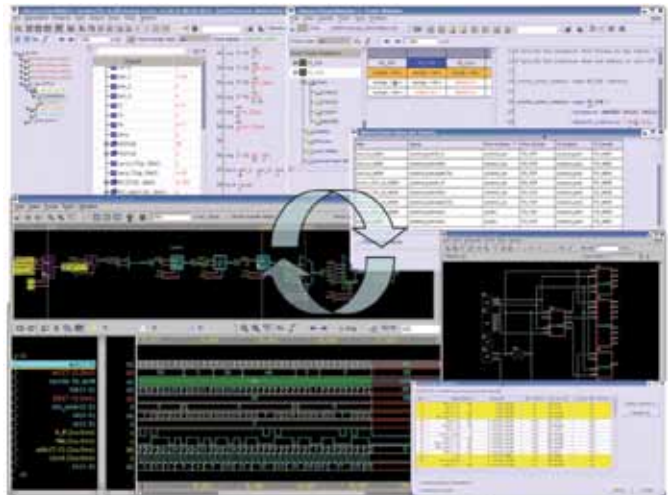
The Verdi™ Power-Aware Debug Module accelerates the comprehension of power intent and automates the process of visualizing, tracing, and analyzing the source of power-related errors. It simplifies the verification of low-power system on chip (SoC) designs with unique automation technologies that help you:

- Visualize power intent with UPF/CPF
- Comprehend impact of power intent on HDL design
- Automate debug to determine whether unexpected design behavior is caused by functional logic or power-related issues

Low Power Debug Challenges

Low-power design requirements add more complexity to an already burdened verification process. RTL design can represent function and timing, but not power states. Gate-level design includes all information but the verification is too tedious. IP reuse is not possible when power requirements change. The need for a consistent format for describing power intent across the entire design and verification methodology creates new challenges that:

- Introduce the new PDML language into the verification flow (UPF/CPF)
- Require power aware design environments to understand the power specification in the HDL design
- Create a gap between HDL debugging and power-aware debug tools



Power Intent Comprehension

The Verdi Power-Aware Debug Module provides a high-level overview of power intent that can be correlated with RTL design data for a complete power-aware understanding of designs.

Core features include:

- Full UPF and CPF source code support allows you to import and compile power design data into FSDB
- Easy-to-use Power Manager browser enables you to:
 - > Visualize power domains, power networks and power states/modes
 - > Annotate power intent on all design views (nTrace, nSchema and nWave)
 - > Locate power-related constraints for each power domain (power switch rules and retention, isolation and level-shifter rules)
- Drag-and-drop cross-probing between PDML and all design views to identify the origin of power-related problems

Power-Aware Debug Automation

Using the automated HDL debug capabilities of the Verdi system, you can track down the root cause of power-related design behavior across HDL design and power domains. Core features include:

- Automatic unrolling of signal paths driven by power intent across different power domains back to the source code origin
- Automatic tracing to locate drivers/loads across the Power Manager and all design views
- Active annotation of dynamic power modes in both the Power Manager and all design views for seamless tracing between HDL and CPF/UPF code
- Temporal Flow View of power circuits that shows retention registers with save/restore signals and enables you to automatically trace control signals
- Power State monitors that automatically identify the current power status of any signal at any simulation time

- Special visualization for the values caused by power intent rules, such as isolation rules and power on/off
- Reporting of signals impacted by power intent and related from/to instance (driver/load) with power domain
- Automatic list X of selected signals with its driver and related power status

Bridging the Power Verification Gap

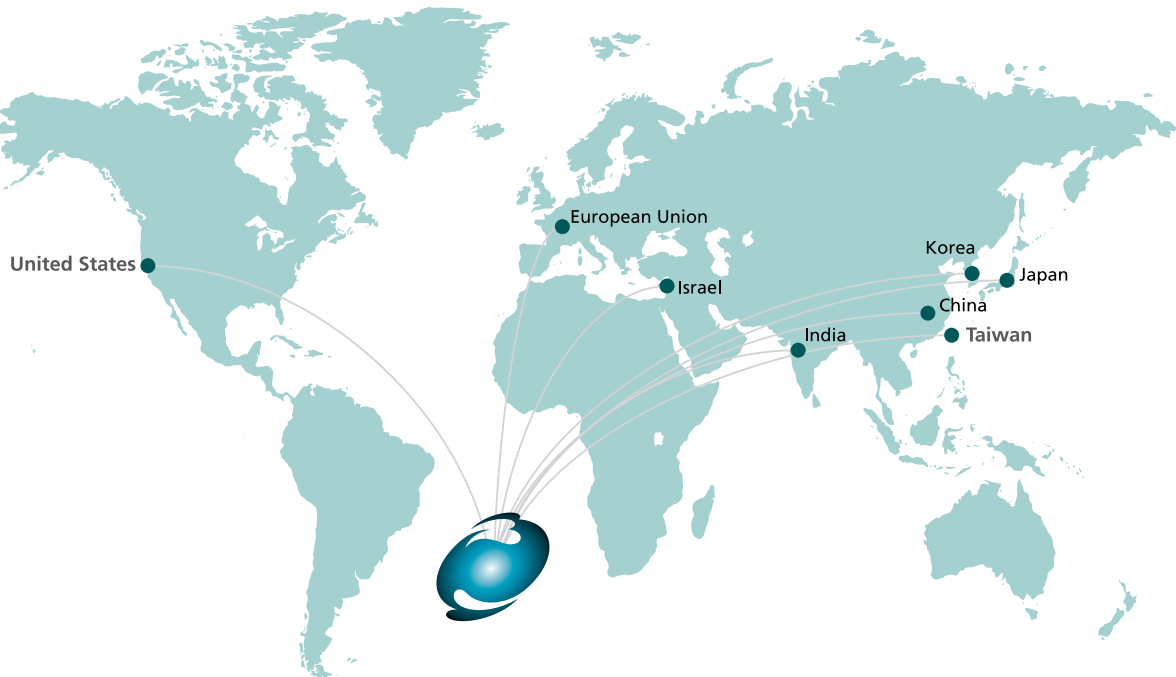
The Verdi Power-Aware Debug Module bridges the power verification gap with a universal platform for integrating power formats and innovations with HDL debug automation. By making it easier to visualize, trace and analyze complex power behaviors in both HDL design and UPF/CPF code, power issues can be resolved earlier in the process while also saving valuable verification cycles.

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