

# ProtoLink Probe Visualizer

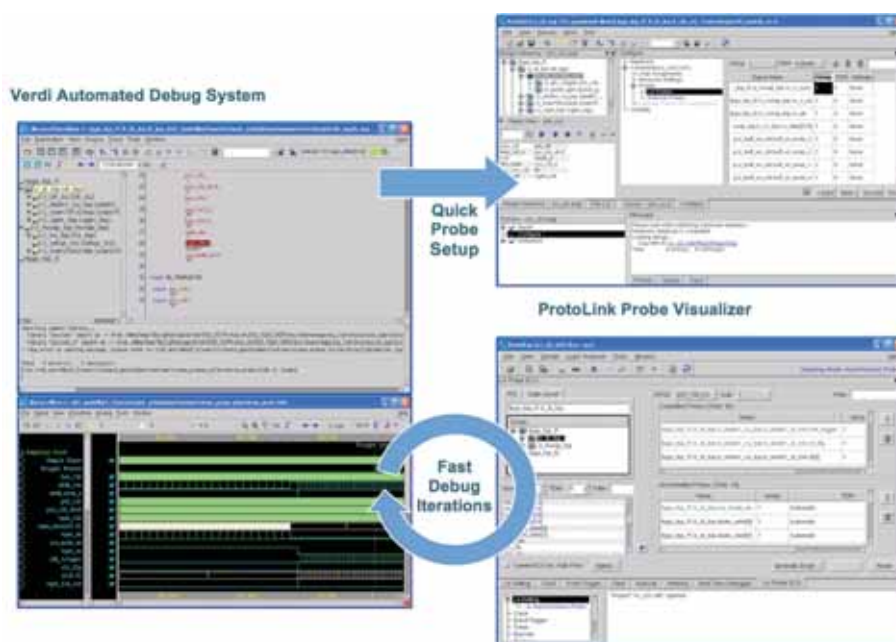


## FUNCTIONAL CLOSURE SOLUTIONS

The ProtoLink Probe Visualizer is an innovative prototype verification solution that dramatically increases design visibility and simplifies debug of off-the-shelf and custom-designed FPGA-based boards.

Probe Visualizer allows you to:

- Cut prototype debug time in half
- Improve verification efficiency for early validation of SoC designs
- Maximize ROI with faster and earlier deployment



## Accelerate Prototype Board Verification

Probe Visualizer uses patented interconnect technologies and specialized software automation to bring the power of SpringSoft's industry-leading Verdi™ Automated Debug System to the prototype board. This unique combination creates a new paradigm for rapid prototype verification that enables board developers and SoC design teams to:

- Gain real-time visibility into thousands of signals for millions of cycles
- Debug designs on prototype boards at the register transfer level (RTL)
- Add/change probes in just minutes with fast ECO flow
- Seamlessly debug pre-partitioned designs across multiple FPGAs

FUNCTIONAL CLOSURE SOLUTIONS

## Increase Design Visibility

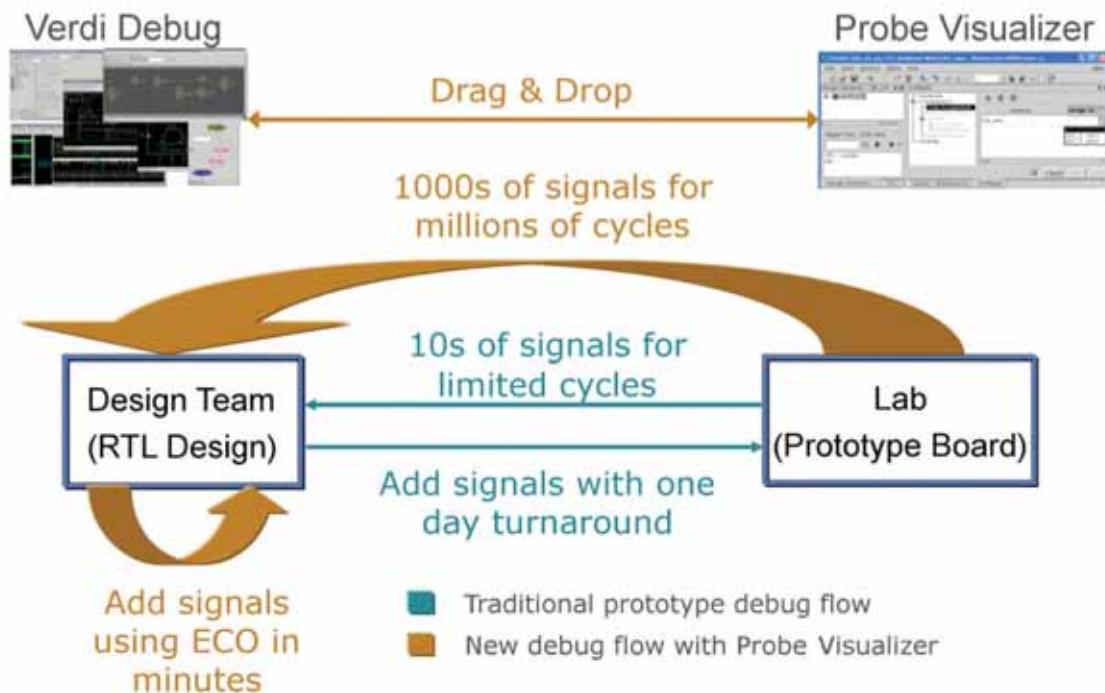
Probe Visualizer provides a flexible FPGA prototype verification methodology that overcomes the limited visibility, ease of use and cost barriers of traditional hardware-assisted approaches. It uses intuitive, software-based methods to achieve a high level of design visibility that:

- Expands number of probe signals from 10s to 1000s with user-friendly time-division multiplexing (TDM) technology
- Supports multiple probe groups and probe buses for viewing up to 8K signals per FPGA per probe bus at one time
- Deploys Siloti Visibility Automation System, if desired, to determine minimum set of probe signals needed for optimal design visibility

## Reduce Debug Turnaround Time

Probe Visualizer makes FPGA prototype boards easier to debug starting at the RTL design stage all the way through final implementation. It shares the same compiling technology and knowledge database as SpringSoft’s Verdi debug platform to:

- Ease RTL debug with advanced visualization, tracing and analysis capabilities
- Drag-and-drop probe signals between Verdi and Probe Visualizer environments
- View waveforms and set event/triggers across multiple FPGAs to analyze design behavior and identify the root cause of bugs
- Add/modify probes with partial routing to eliminate long recompile and debug loops
- Maintain RTL-to-gate correlation throughout prototype debug flow



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FUNCTIONAL CLOSURE SOLUTIONS

## Comprehensive, Easy to Use

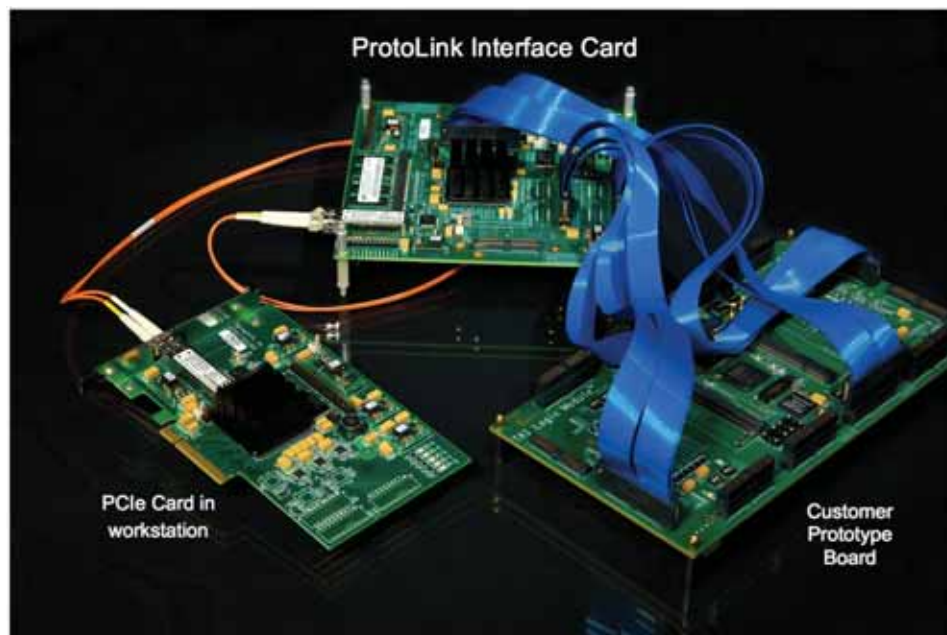
Probe Visualizer automates FPGA setup, probe instrumentation, and interface tasks. Its hardware-independent architecture enables out-of-the-box operation with custom or off-the-shelf prototypes and eases the transition to next-generation boards with the latest FPGA technologies.

### Core Features

- Synchronous and asynchronous sampling with small footprint soft IP on each FPGA
- Probe data captured and uploaded into SpringSoft FSDB for debugging
- Single design compilation to use Probe Visualizer and Verdi debug software
- Probe Memory stores up to 44 million cycles without using FPGA resources
- Probe ECO with integrated revision management system saves hours of setup time
- Flexible hardware kit links prototype board with engineering workstation to run conventional in-circuit emulation

The ProtoLink Hardware Interface kit provides:

- ProtoLink Interface Card to bridge the workstation running the Probe Visualizer software to the prototype board via standard J-connectors or Mictor connectors
- High-speed Fibre channel for connecting the interface card to the workstation
- 2GB Probe Memory on the interface card to store probe data
- Support for custom prototypes and pre-fabricated HAPS System, TAI Logic Module, and Chiplt boards



For more details about the underlying innovations and use model enabled by the ProtoLink Probe Visualizer, download the technology background at:

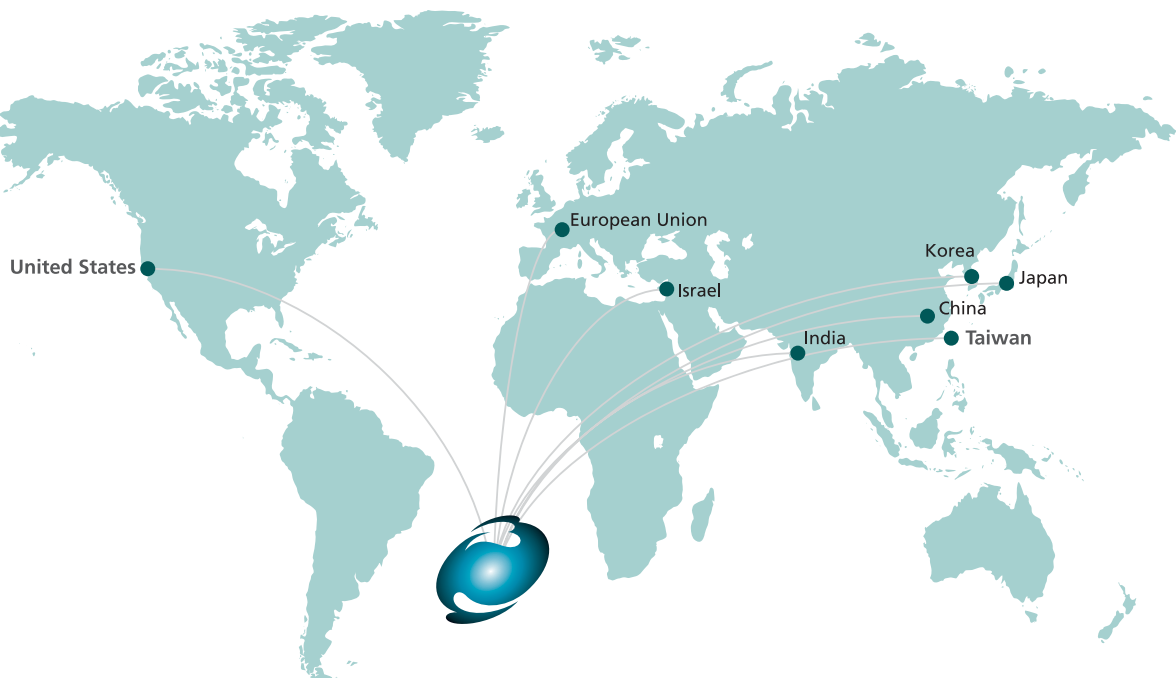
<http://www.springsoft.com/technology/technical-papers/verification-technical-papers/probe>

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