

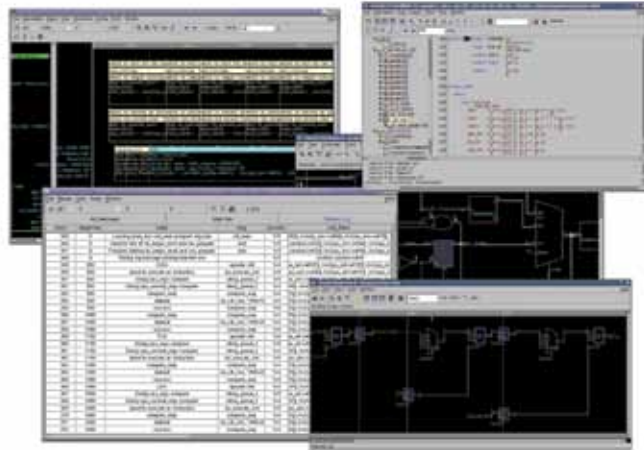
Verdi™ Automated Debug System



VERIFICATION ENHANCEMENT SOLUTIONS

The Verdi™ Automated Debug System is an advanced solution for debugging digital designs that provides powerful technology to help you:

- *Comprehend* complex and unfamiliar design behavior;
- *Automate* difficult and tedious debug processes; and
- *Unify* diverse and complicated design environments.



The unique behavior analysis technology of the Verdi system automates many time-consuming aspects of debug.

Cut Debug Time in Half

The Verdi system lets you focus on tasks that add more value to your designs by cutting your debug time, typically by over 50%. These time savings are made possible by unique technology that:

- Automates behavior tracing with its unique Behavior Analysis technology;
- Extracts, isolates, and displays pertinent logic in flexible and powerful design views; and
- Reveals the operation of and interaction between the design, assertions, and testbench.

Complete Debug System

The Verdi Automated Debug System incorporates all of the technology and capabilities you would expect in a debug system. In addition, the Verdi system combines advanced debugging features with support for a broad range of languages and methodologies.

Core Features

The Verdi system provides the following fundamental debug features:

- *Full-featured Waveform Viewer* enables you to display and analyze activity over time
- *Powerful Waveform Comparison Engine* allows you to isolate differences between Fast Signal Database (FSDB) files
- *Source Code Browser* enables you to easily traverse between source code and hierarchy
- *Flexible schematics* and block diagrams give you the ability to display logic and connectivity using familiar symbols
- *Intuitive bubble diagrams* help you to reveal the operation of finite state machines

Advanced Features

The Verdi system also includes the following advanced debug features:

- *Automatic tracing of signal activity* enables you to quickly trace activity across many clock cycles with powerful behavior analysis technology
- *Temporal flow views* provide a combined display of time and structure to help you rapidly understand cause-and-effect relationships
- *Transaction-based debug* with flexible transaction and message support for debugging and analyzing designs at higher levels of abstraction
- *Assertion-based debug* with built-in support for assertions facilitates quick traversal from assertion failure to related design activity
- *SystemVerilog testbench debug* with:
 - > Full source code support for SystemVerilog Testbench (SVTB) and libraries including Universal Verification Methodology (UVM) to ensure reusability and interoperability of testbench code
 - > Specialized views that help you to understand testbench code, including declaration-based hierarchy browsing and navigation, class inheritance and relationship comprehension, and tracing
 - > Built-in message logging and automated UVM transaction recording capabilities, coupled with advanced visualization techniques, give you a complete picture of testbench activity in the post-simulation verification environment
 - > Full-featured interactive simulation control allows you to step through complex testbench code for more detailed analysis

Languages and Methodologies

The Verdi system supports the following languages and methodologies:

- Design components described in Verilog, VHDL, and SystemVerilog
- Automated testbench environments using SVTB as well as UVM, OVM and VMM
- Assertions using SystemVerilog Assertions (SVA)

Optimized Open Architecture and Unified Methodology

The Verdi Automated Debug System is designed so that you can take full advantage of your verification and debug methodology. The Verdi system is built on the open Design Knowledge Architecture, which consists of compilers that extract relevant information into databases that are optimized for efficient debug. The Verdi system also unifies your debug process by providing a single solution that operates seamlessly and consistently across multiple domains — verification tools, design/verification languages, and abstractions. This consistency reduces your learning curve and saves time as you move to new projects using different tools and languages, and allows you to further leverage your investment in the Verdi system even as your other tools and methodology evolve.

The Design Knowledge Architecture is comprised of the following:

- Knowledge Engine Compilers extract design knowledge contained in HDL code, testbenches, and assertions
- Knowledge Database(KDB) stores crucial design knowledge to facilitate debug and understanding of your design
- Fast Signal Database (FSDB) captures and stores results from simulators, emulators, and formal tools that produce time/value sequences
- Application Programming Interfaces (APIs) provide open access to both databases and command-and-control mechanisms, enabling you to easily integrate the Verdi system with other verification tools and design environments

Interoperability

The open architecture of the Verdi system allows for easy integration with both commercial and proprietary verification tools. Through an ever-expanding list of partners, the Verdi system provides you with a fully integrated, predictable environment with out-of-the-box support for a wide range of commonly used commercial tools, including:

- Simulators
- Emulators and accelerators
- Model checkers and other formal analysis engines

Debug and Analysis Across Multiple Abstraction Levels

The Verdi system further unifies comprehension by allowing you to seamlessly debug throughout your methodology flow from System level to Gate-level verification. The Verdi system provides additional support for verification and analysis at the implementation level with the nAnalyzer Design Implementation Analysis module. The nAnalyzer module provides a single environment for analyzing troublesome design errors related to clocks, clock trees, and timing.

Debug of Power-Aware Design Intent

The Verdi system is also available with the added Power-Aware Debug Module to accelerate the comprehension of power intent and automate the process of visualizing, tracing, and analyzing the source of power-related errors. The Verdi Power-Aware Debug Module simplifies the verification of low-power system on chip (SoC) designs with unique automation technologies that help you:

- *Visualize* power intent with UPF/CPF
- *Comprehend* impact of power intent on HDL design
- *Automate* debug to determine whether unexpected design behavior is caused by functional logic or power-related issues

The Verdi Automated Debug System Saves You Time

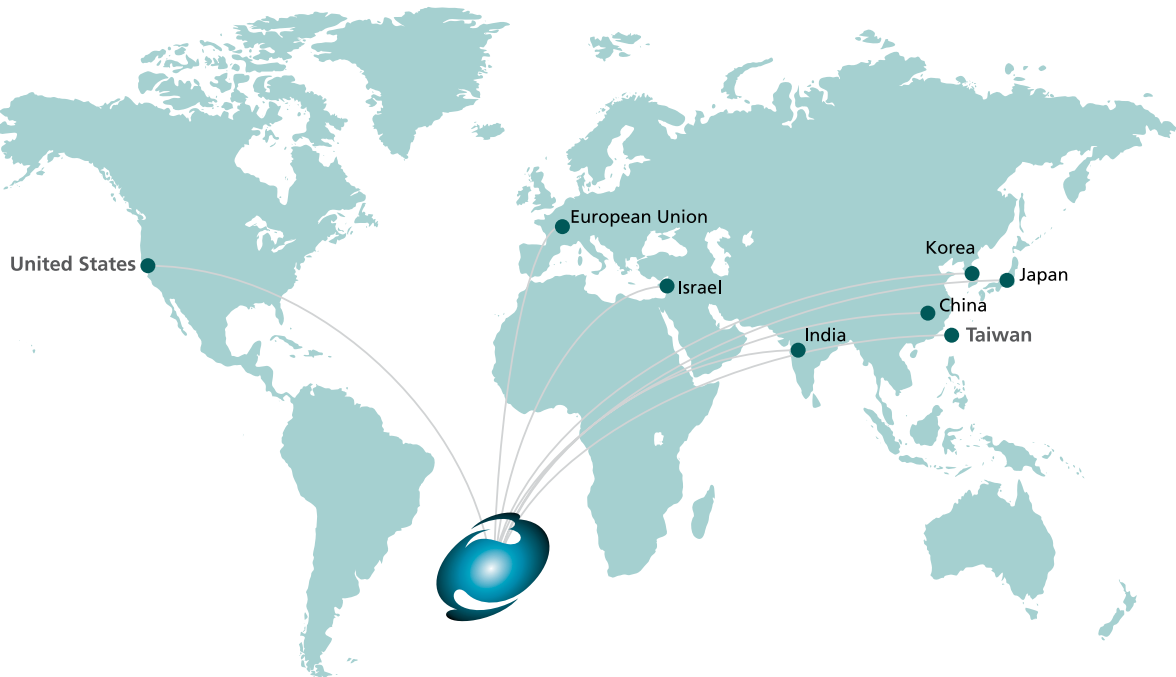
The Verdi Automated Debug System is an award-winning debug platform that cuts your debug time in half. This robust and sophisticated system significantly reduces the time and effort required to comprehend the behavior of complex designs by eliminating tedious and manual tasks. The Verdi system's open architecture and extensive integration with popular commercial tools unify your verification environment for even greater efficiency. With over 400 customers and 60 EDA partners, the Verdi system has become the industry's de facto standard debugger. Our customers tell us that the time they saved using the Verdi system has given them more time to add greater value to their designs, work on other job-related tasks, and enjoy more personal time. At SpringSoft, our mission is to accelerate engineers. The Verdi Automated Debug System is one way that SpringSoft is Accelerating Engineers.

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