



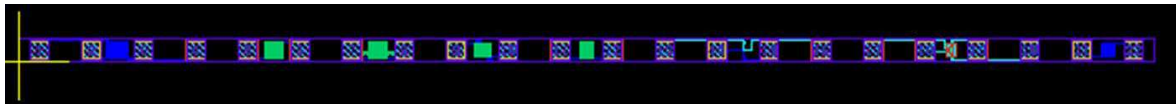
Laker T1 Test Chip Development System

Overview

Test chips play a pivotal role in semiconductor process development. A properly designed test chip pushes the limits (corners) of the manufacturing process in order to define the boundaries or “process window” that offers the highest production yield. Test chips are the qualification vehicles used to bridge the gap between process simulation and production yield and they can have a dramatic impact on the time-to-market for new technologies. Unfortunately, there never seems to be enough time in the schedule to develop and document a really comprehensive test suite that will give the kind of process feedback that device and process engineers need. This is made even more difficult during process development while the new process is constantly changing.

After a process is qualified, test lines are typically placed between chips on production wafers in order to continually monitor production processes. In a world where customization is king, derivative processes – even as simple as different numbers of metal layers – also benefit from the rapid turnaround of production test line monitors. Creating and maintaining a large library of custom test lines for derivative processes can become a maintenance nightmare.

The Laker™ Test Chip Development (TCD) system addresses these issues with a unique and dedicated platform for test chip development that dramatically reduces technology time-to-market. The Laker TCD system was developed by SpringSoft in conjunction with top-10 semiconductor manufacturers and is used by companies in every major semiconductor market.



Superior Test Chips with Less Effort

The Laker Test Chip Development system is uniquely focused on test vehicle development to save time at a critical point in process development. It provides an intuitive user interface for creating reusable parameterized test structure and test line libraries. Parameterizing structures that are typically hand-drawn allows you to create an almost infinite number of layouts from a single structure by assigning variables to key drawing dimensions. With the Laker TCD system, you are able to change from the tedious and error-prone conventional test chip development flow to an efficient, consistent, and automated methodology.

- **Reduce test chip development cycle time** from months to weeks or days vs. conventional test chip development methods
- **Speed up** time-to-market for new technology development, process transfer, and ramp to production
- **Reduce process development costs** with fewer mask-set and wafer respins by removing the guesswork of manual test chip layout and documentation. Parameterized test line architecture

provides true scalability and reusability across multiple technology nodes and process varieties offering:

- Additive time savings through knowledge re-use;
 - The flexibility to respond to last-minute process changes or to quickly enable process derivatives by adjusting test structure parameters and,
 - The ability to generate large numbers of variants to obtain higher quality process data with little impact on throughput or development cost.
- **Simplify the test line generation process.** Once the parameterized libraries are in place, test chips and test lines can be implemented by process technologists rather than layout designers
 - **Save time after tapeout.** Automated document generation not only offers rapid and accurate documentation delivery but also saves time downstream for probe, test and device engineering teams

Major Features

The Laker T1 Test Chip Development process consists of 4 major steps. Each step leverages the previous steps through automation, accumulating value at each level.

Step 1: Create parameterized test structures and devices

Step 2: Create parameterized testlines by defining the probe line (pad arrangement) template; placing the chosen parameterized test structures; and assigning connectivity.

Step 3: Create the split table of parameters and realize (generate the layout), route and document the actual test lines.

Step 4: If assembling the test lines into larger arrays of test lines: Assign test line locations in the chip assembly module to create test chip blocks and final GDS2 layout.

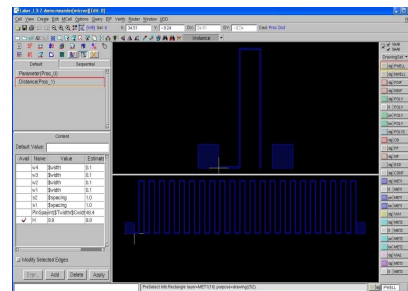
Steps 1 and 2 are embodied in the TestLine Manager module and steps 3 and 4 are part of the Test Line Realizer module, described below.

Test Line Manager

The *Test Line Manager* consists of 4 major components, the *Test Structure Compiler*, *Parameterized Test Structure Library*, *Probe Line Editor*; and *Test Line Editor*. The function of the Test Line Manager is to prepare parameterized test lines.

Test Structure Compiler

The *Test Structure Compiler* is the knowledge engine that captures the “master” test structures and assigns parameters to their flexible elements, creating parameterized test structures (PTS). The PTS can be as simple as a metal plate, a Kelvin contact, or a transistor, and can be as complex as a variable via chain, a differential pair or even a ring oscillator. The flexibility of each PTS comes from the parameters you define; the only limitation is human capacity to manipulate the various parameters. For example, once a master test structure is properly parameterized, it only takes a few mouse clicks to change a 3-by-5 via1 chain to a 6-by-12 via2 chain.



The *Test Structure Compiler* supports three input mechanisms:

- Creating new PTS using the Laker TCD GUI
- Hand-coding new PTS using Tcl scripts

- Importing and parameterizing GDSII data of existing test chip structures from legacy test chips.

Parameterized Test Structure Libraries

PTS are stored in the PTS library, a central repository of all test chip information which allows you to restrict access to sensitive process information, enabling corporate-wide technology knowledge management and worldwide intellectual property control.

SpringSoft supplies a generic test structure library in Laker TCD that contains a set of PTS whose designs are generally available in the public domain. The library covers basic test structures for testing sheet resistance, contact/via resistance, opens and shorts, electromigration, junction characterization, thin dielectric, single devices, antenna effect, and matching and ESD devices. This generic library is SpringSoft property but is available to Laker TCD users for internal use to modify and deploy.

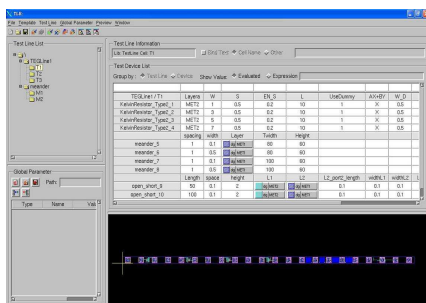
Probe Line Editor

The *Probe Line Editor* is an interactive graphical user interface that enables you to specify the configuration of the probe pads. It delivers a flexible template that allows you to adjust the pad alignment, including single row, multi-row or ring type pad arrangements. You may also create custom pad arrangements and/or employ multiple pad cells by specifying coordinates and cell names. Engineers are able to quickly shrink the probe card pad pitch and effective scribe line width with little effort, increasing the die per wafer when narrower scribe lines are available.

Test Line Editor

Using the *Test Line Editor* you create the test lines by placing devices from the PTS library in the probe lines and specifying connectivity. An easy-to-use preview editor allows you to try out various combinations of probe lines and PTS.

Test Line Realizer



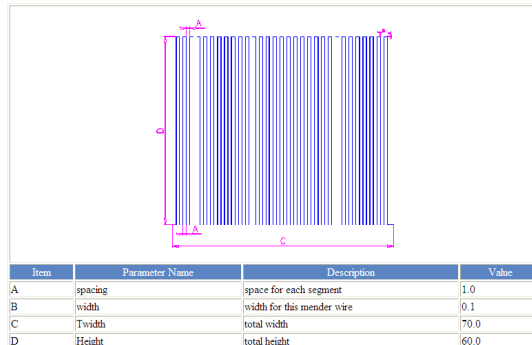
The *Test Line Realizer* is the core of the Laker TCD system. It manages and compiles all master test lines into actual layouts and corresponding documents. You can quickly assign split tables for any parameter of interest using a spread-sheet-like user interface. The *Test Line Realizer* employs a unique routing algorithm that is custom-tailored for test chip routing including such things as tapered and mesh interconnects. Automated layout creation provides accuracy and quality that is a world beyond any manual layout approach.

Laker layout

Laker TCD includes much of the functionality of the Laker layout tools. The layout editor enables you to lay out specialized devices and assemble test chips with a mixture of IP, library development modules, and test lines. It enables review and verification of created test lines using integrations with both 3rd-party physical verification tools and simple hand-measurements. A built-in pathfinder router is available for top level routing, and Laker Mcell™ technology is available for automated guard-ring generation and contact/via stacks for the routers.

Document and Netlist Generator

The automated *Document Generator* saves a lot of time in tedious (and likely inaccurate) document generation. It offers a graphic notation interface that enables you to easily document the PTS parameters, making them more maintainable and readable. It then exports the test line documentation automatically including device name, pad assignment, location, test line schematic view and other information. At the same time, the *Netlist Generator* generates a netlist that enables test line LVS verification. When the test lines are complete, the documentation and LVS netlists are also ready to go.



Summary

In today's hyper-competitive semiconductor industry, getting a new technology to market and meeting commitments are basic survival skills. Not only do you have to lead in process development but you also must also ramp to full production quickly and accurately. Test chips have become an essential and critical path item in achieving industry leadership. SpringSoft has applied software automation technology to the test chip design process to expedite process development, production ramp and process monitoring in this fast-moving, constantly changing environment.

Open System

Laker TCD supports complete Tcl/Tk syntax plus some extensions for maximum flexibility in tool customization, database query, and test key creation.

Supported Platforms

Platforms
Solaris SunOS 5.7, 5.8, 5.9, 5.10 SPARC (32bit/64bit)
Linux Redhat 7.2, 8.0, 9.0 (32bit)
Linux Redhat Enterprise 3.0 (32bit/64bit)
Linux Redhat Enterprise 4.0 (32bit/64bit)
HP-UX 11.0 (64bit)

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