

# Deploying Functional Qualification at STMicroelectronics Methodologies & Case Studies



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# Agenda

## **Motivation and history**

- ◆ Initial engagement
- ◆ Deployment of functional qualification within ST

## **Functional Qualification Methodology @ ST**

- ◆ Use Models & Methodology
- ◆ Sharing Best Practices within ST
- ◆ Detection Strategies
- ◆ Future directions

## **Case studies**

- ◆ Measuring 3rd party IP Quality
- ◆ Detection strategy on a Video Codec



# ST & Certess - Motivation and history

- ❏ **Code & Functional Coverage were not enough**
  - ◆ Only measures capacity of stimuli to exercise the design
  - ◆ Nothing guarantees proper verification of covered areas
- ❏ **Interest of Mutation-Based Technology was obvious**
  - ◆ Filling a major hole in functional verification
  - ◆ First objective metric to measure functional correctness
- ❏ **Started to collaborate with Certess in 2004**
  - ◆ Service model – on Certitude prototype
  - ◆ Very promising results
    - ▶ Highlighted verification environment weaknesses



# Deployment

## **Main factors of Certitude adoption**

- ◆ Capable to cope with heterogeneous environments, non-intrusively
- ◆ Quality gains: first objective measure of functional correctness
- ◆ Productivity gain: help to focus verification efforts
- ◆ Tool robustness & ease of use

## **Limitations**

- ◆ CPU Time Consumption
- ◆ Analysis of results: from Non Detected fault to bug
- ◆ Methodology was missing to maximize R.O.I on qualification runs

## **Deployment**

- ◆ Limitations reduced with proper methodology
- ◆ Now covering 80% of ST's IPs
- ◆ Certitude Metrics are our most important verification completeness indicators
  - ▶ Code coverage has been replaced by Activation ratio



# Certitude Use Models

## ■ Mean to measure the functional completeness of Verification Environments (thus of IP)

- ◆ **Certitude-Metric** mode
- ◆ Criterion to know on which IP to focus verification effort
- ◆ Criterion to select an IP provider

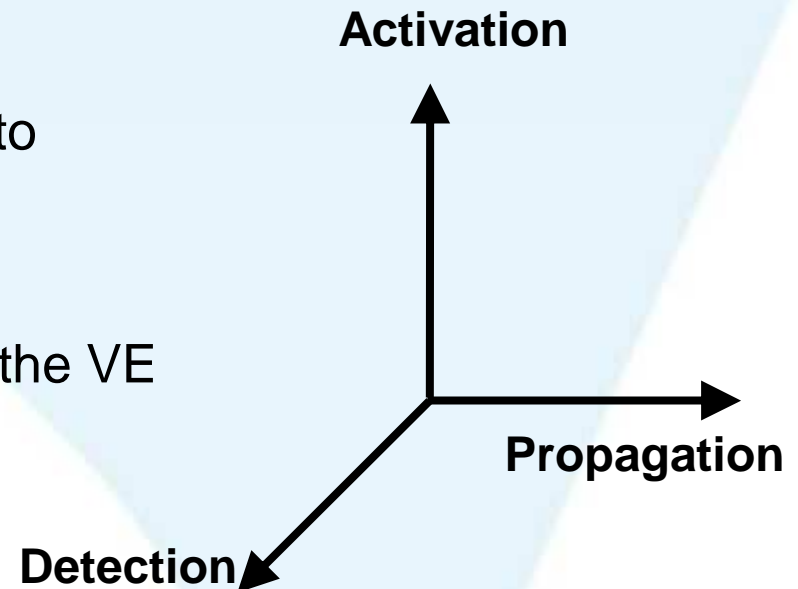
## ■ And to improve quality of Verification Environments, thus of IPs

- ◆ **Certitude-Improvement** mode
- ◆ Many RTL bugs found using this technology
- ◆ Detection Strategy is key to reduce CPU consumption and ease results analysis



# Certitude Metric Mode - Global Quality Indicators

- **Certitude provides 3 orthogonal quality metrics**
- **Activation score (A/F)**
  - ◆ Quality of Stimuli and their ability to control mutations
- **Propagation score (P/A)**
  - ◆ Quality of Stimuli and their ability to observe mutations
- **Detection score (D/P)**
  - ◆ Quality of the checking system in the VE
- **Global metric (D/F)**
  - ◆ Figure summarizing all.



# Deploying best practices within ST

## **Verification cockpit**

- ◆ Factorization of the setup of all verification tools

## **Internal Qualification Workshop focusing on**

- ◆ Detection Strategy
- ◆ Results Analysis

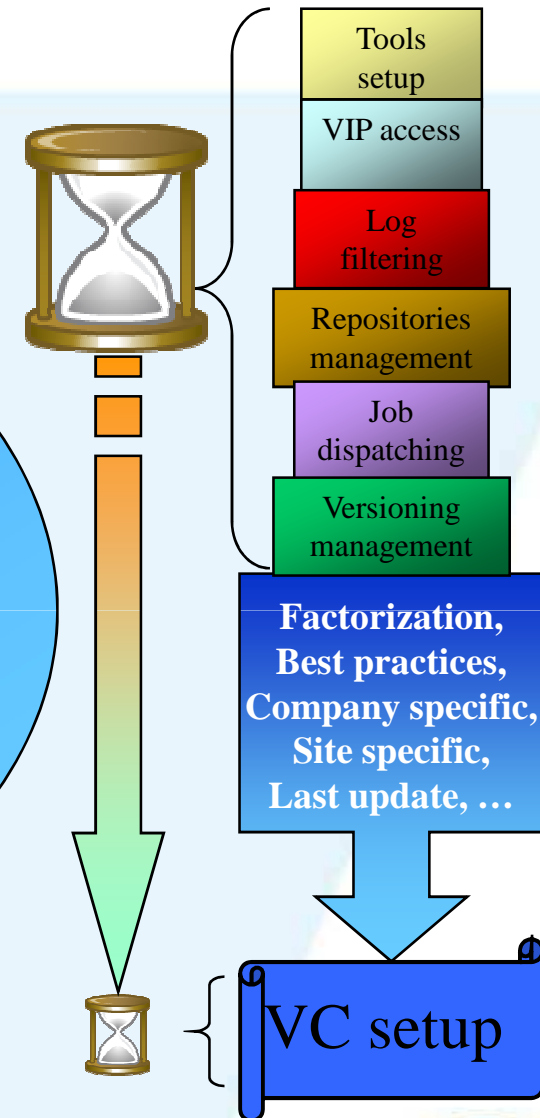
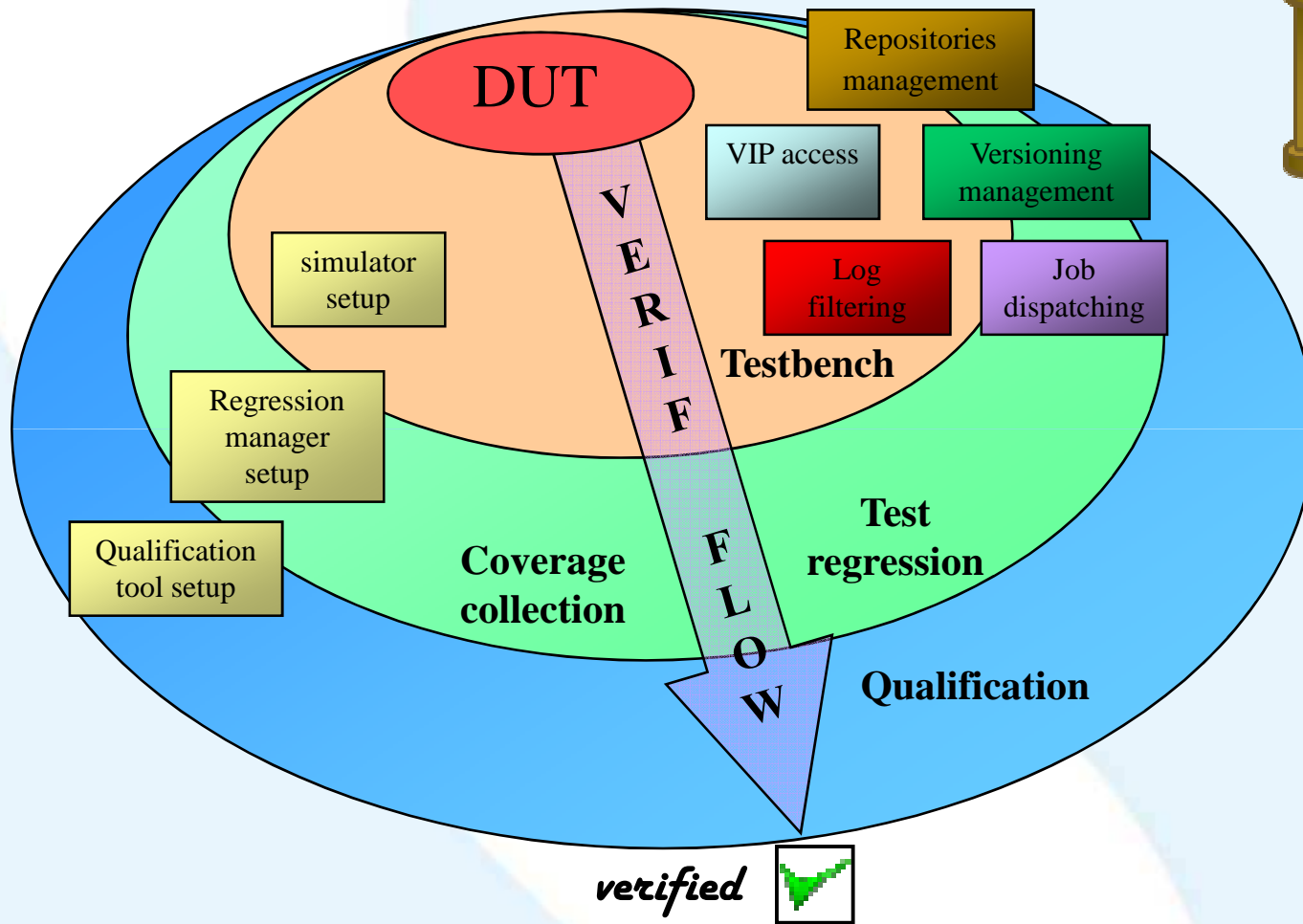
## **Knowledge Sharing**

- ◆ Certitude User's Group run Quarterly in ST
- ◆ Intranet portal :
  - ▶ Document, Bug trackers, Mailing list, Wiki, Subversion



# Verification Cockpit

## Productivity gains in setup



# Verification Cockpit

## Benefits for Certitude Users

### **Robustness and of the certitude\_execute**

- ◆ Encapsulation of workarounds to LSF and Clearcase common issues
- ◆ Tolerance to IT stability issues (efficient use of retry)

### **Central maintenance**

- ◆ No certitude\_execute to write !
- ◆ Benefits of best practices and avoid common mistakes (eg. End of test)
- ◆ Reduce need for support

### **Usage of advanced features**

- ◆ Checker Analysis
- ◆ Status History
- ◆ Metric collection script
- ◆ Certess's Hierarchical Dropping & Incremental Detection (aka HBID)
- ◆ Analysis hints scripts



# Methodology evolution - future

## Usage of Certitude to measure “assertion density”

- ◆ Prototype Certitude & IFV integration already in Verification Cockpit
- ◆ Experimented on two blocks with very encouraging results
- ◆ Mutation Based Metrics becomes a common metric for formal & dynamic

## Certitude-C

- ◆ To qualify ‘C’ reference models and HLS models

## Integration within Cadence’s Enterprise Manager

## Linking mutations to functionality and verification plan



# Case studies

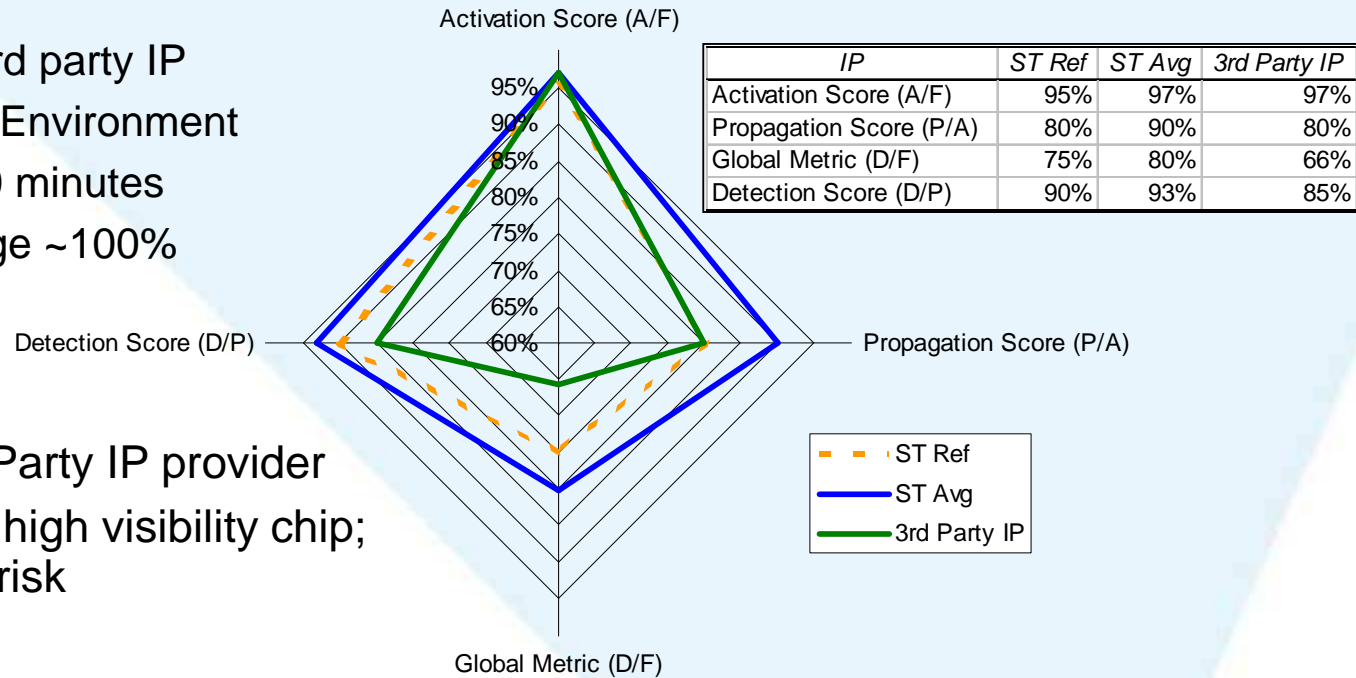
- **Following are a few case studies that illustrate two kinds of environments we are running**
  - ◆ Case study 1: Third-party IP qualification
  - ◆ Case study 2: Video Codec Incremental Qualification



# Case study 1 : 3rd Party - IP qualification

- **Case study 1:**

- Application: 3rd party IP
- HDL Directed Environment
- ~300 tests, 30 minutes
- Code Coverage ~100%



- **Challenges**

- Convince 3rd Party IP provider
- High revenue, high visibility chip; reduce respin risk

- **Results**

- Helped us to push IP provider to improve verification environment
  - and monitor progress
- Low detection score highlighted manual waveform checks



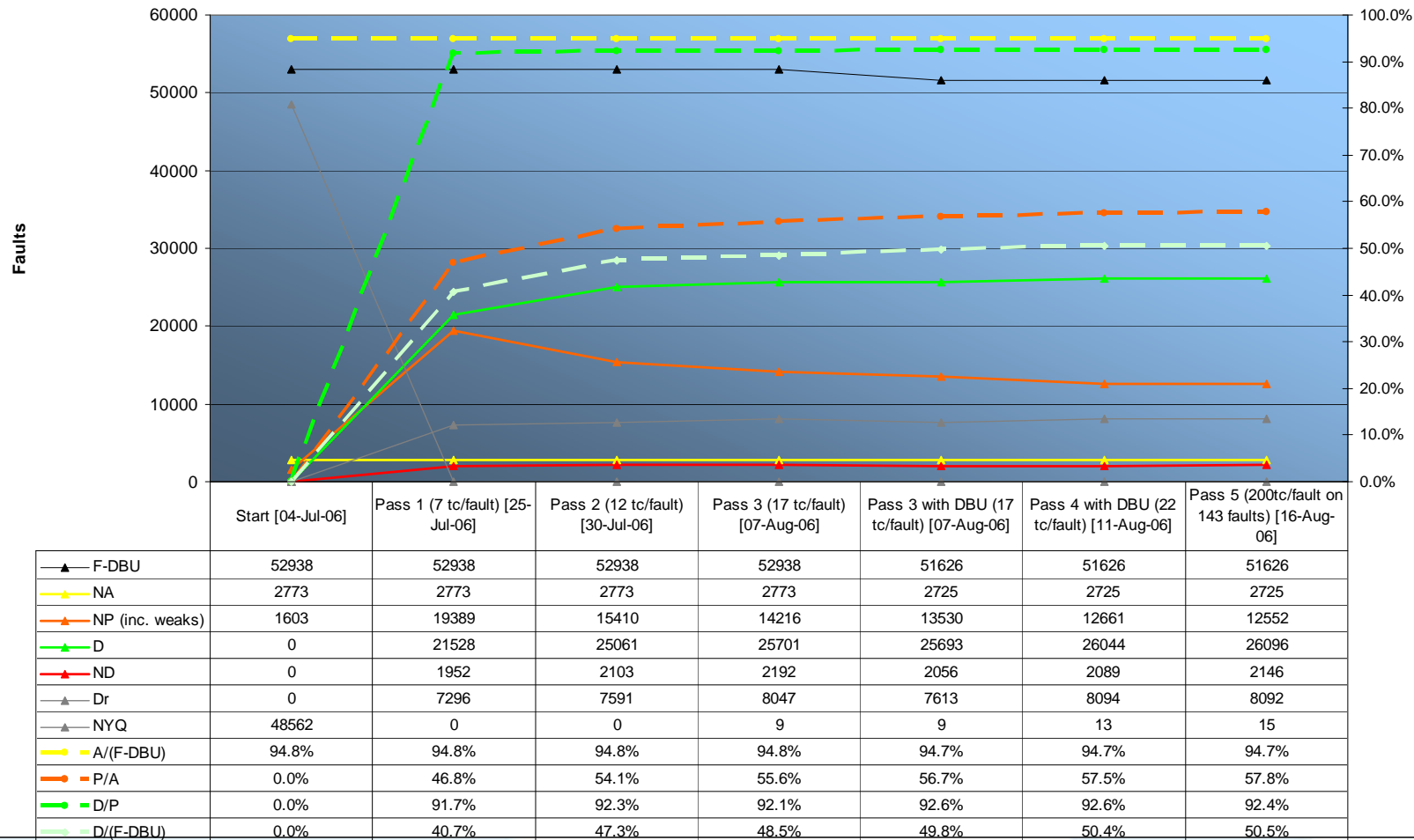
# Case study 2 : Video Codec

- **Case study 2:**
  - Application: Video CODEC
  - 1.5 Millions Gate
  - 23000 tests considered
  - Experiment done in 2006
- **Challenges**
  - Scalability : very complex IP with very long regression suite
  - Full Detection was out of reach for this IP and detection strategy needs to be adapter
- **Results**
  - One major weakness in the verification environment was highlighted
  - “Detection Strategy” was born, hierarchical dropping & incremental detection
- **Environment**
  - SystemC-TLM platform
  - Regression: ~1 CPU year



# Case study 2 : Hierarchical Dropping

## Evolution through passes



# Summary

- **Functional Qualification introduction over the last 3 years had major benefits**
  - ◆ Major increase in overall chips quality
  - ◆ Good productivity increase in verification process
  - ◆ Objective and common metrics
- **Methodology was key to enable these benefits**
- **Lots of potential future applications**
  - ◆ Application to formal methods
  - ◆ Application to C/C++ based models
  - ◆ Industry shared criterion to measure 3rd party provided IPs
- **Missing a competitor to give more credit to the technology ;-)**
  - ◆ Industry should align on a mutation model

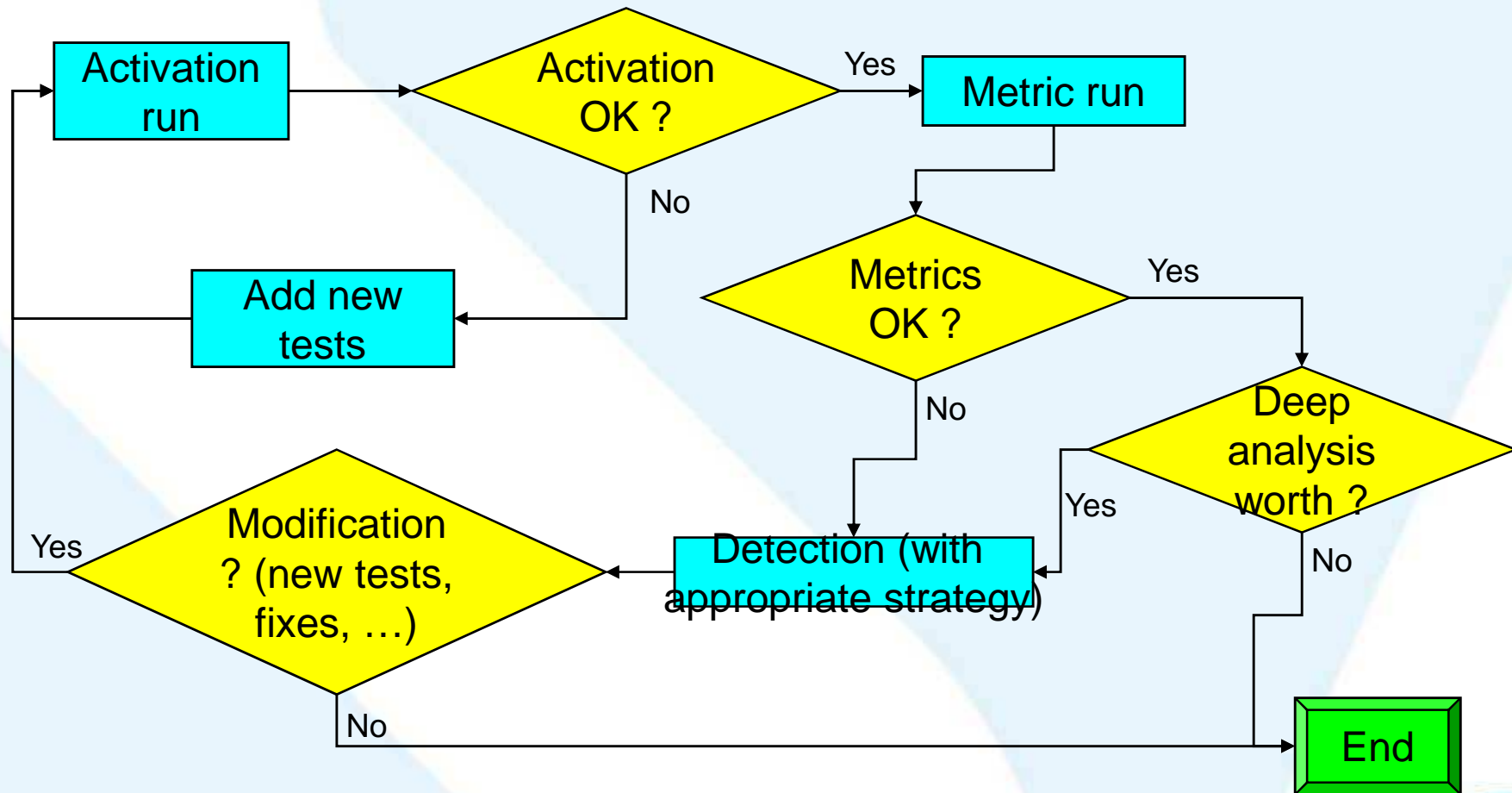


# BACKUP Slides



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# Qualification flow



# Certitude Metrics - ST References

## **Global Metric**

- ◆ Representing the overall quality of the Verification Environment
- ◆ ST reference : 75%, but usually higher

## **Activation Score**

- ◆ Measures the ability of the test suite to exercise all the RTL of the IP
- ◆ Similar to code coverage
- ◆ ST reference : 95%, & 100% explained
- ◆ Missing % should deeply studied & fixed or explained

## **Propagation Score**

- ◆ Measures the ability of the test suite to propagate mutations to the outputs of the IP
- ◆ ST reference : 80%, but should probably be enhanced by adding more test scenarios to reach 90%

## **Detection Score**

- ◆ Measures the ability of the environment to catch errors
- ◆ ST reference : 90%, but usually higher



# When to apply Certitude - present

