

Scaling custom digital layout for next-generation chip design

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Layout for large digital IC designs is generally created using highly automated place-and-route (APR) tools. Although there are trade-offs for using APR instead of custom layout, the speed and confidence offered by APR far out weigh the compromises in area or performance for most designs. But designs that require the utmost in performance and/or the smallest possible area are still done "by hand" using custom IC layout methodologies.

In the next generation of custom chips, complicated rules, tight time-to-market schedules, and the sheer size and complexity of designs are making full-custom digital blocks increasingly difficult to implement. Fully-automated APR flows cannot offer the kind of interactive control of the layout and routing that is necessary. Designers need a highly-automated yet controllable full custom digital IC design flow that optimizes performance, speed and area.

This article details how one digital IC design team at a large fabless semiconductor company in the consumer product market is leveraging standards-based tool interoperability to maintain the benefits of hand layout for large, performance-sensitive 40nm designs. The team has deployed the integration capabilities made possible by the Silicon Integration Initiative's (Si2) Open Access (OA) interoperability standardization effort with tools from multiple vendors to form a more productive custom IC layout flow.

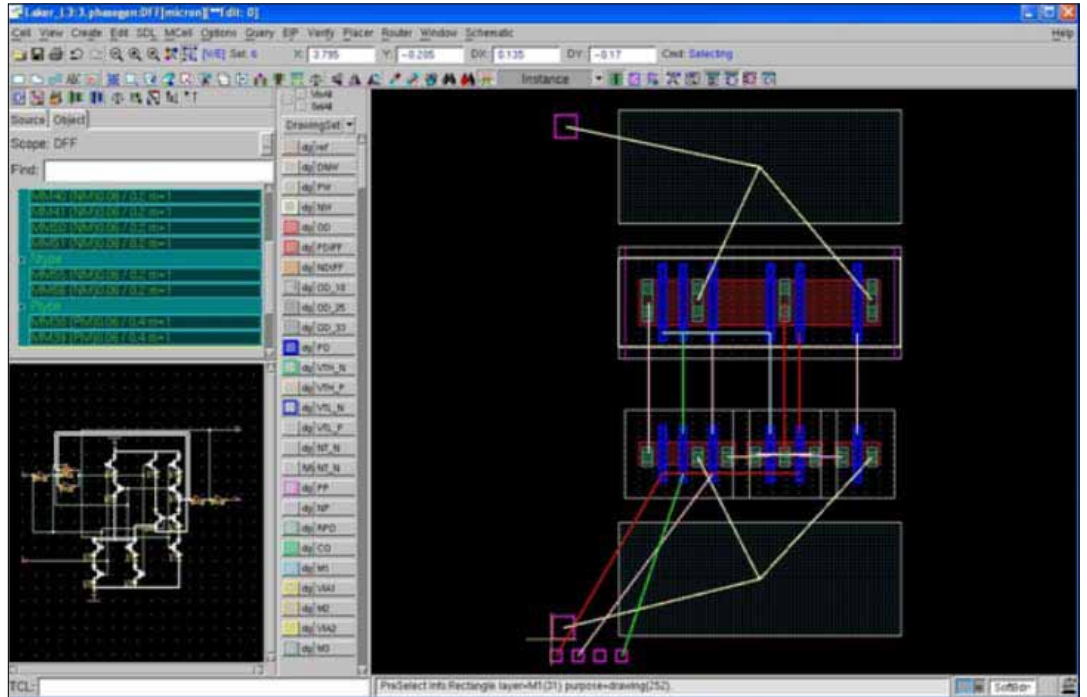


Figure 1: Flight lines show connectivity and guide rule-driven manual routing.

Controllable automation

In designing high-volume storage solutions, the design team has for many years deployed custom IC layout automation for its analog and custom digital designs. While analog designers have always used custom design methodologies, it is typically only when performance, power, speed or area requirements exceed the capabilities of APR tools that digital design teams turn to custom design tools and flows.

For optimal performance and cycle time, engineers use tools that employ advanced controllable automation techniques to create custom digital designs much faster and with less effort. These include an advanced schematic-driven layout (SDL) flow that uses highly configurable, process-independent parameterized cell technology and a device-level floor planning tool that offer the speed and control necessary to achieve the best possible performance and density without having to change design style or compro-

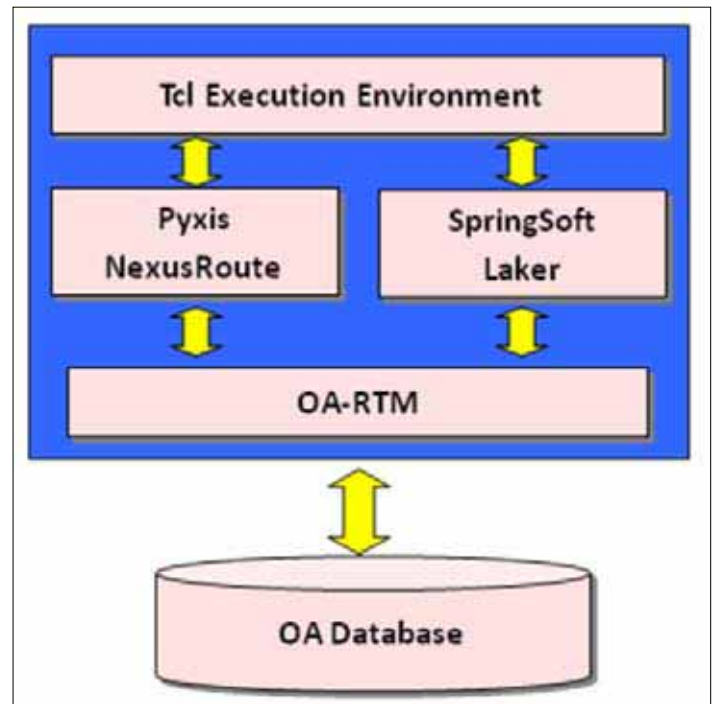


Figure 2: Si2 has made available an interoperable database for EDA tools called OpenAccess (OA).

mise the quality of the result.

Using the flight lines generated from the connectivity automatically carried over from the schematic, the engineers then use

the built-in rule-driven interactive router to wire critical nets by hand to meet demanding clock rate requirements that exceed 2GHz. At this performance level,

painstakingly-drawn critical nets, requiring extensive hand edits or yet another cycle through the router, or possibly both. As a result, the design team spent six weeks moving the design back and forth, in order to converge on an acceptable, albeit sub-optimal, result.

Automated routing, even for non-critical nets, might have improved the team's productivity had it not impeded their ability to work iteratively. Also, there was no way to represent partial pre-routes and the sophisticated spacing constraints needed to guide the APR tools. This, in turn, led to bad parasitic interactions within the custom blocks that required laborious manual re-routes and multiple lengthy re-runs.

While automation typically improves productivity, in this case, it made a difficult process longer because designers could not control the results. Indeed, hand-edits of critical nets in a fully routed layout can take longer than routing by hand initially. The team concluded that in order to achieve optimum results in less time it would require a heterogeneous environment that maintains hierarchy, connectivity and design integrity through controllable automation.

Interoperability saves the day

The standards organization Si2 has made available an interoperable database for EDA tools called OpenAccess (OA) that has in recent years become the standard for custom design. A little-known feature of OA is the OA Run Time

Model (OA-RTM) that can be used when running natively on OA as the in-memory model for EDA tools. This means that entirely different tools may operate on the same in-memory representation of the design data at the same time. Tools from multiple vendors that use the OA-RTM can work as seamlessly together as tools from a single vendor.

Using OA-RTM, a new high-performance custom router from Pyxis Technology is able to work within the design team's existing Laker custom layout environment running on OA. This very high capacity custom digital router is customer-qualified to create DRC-correct, DFM-aware routes at 45nm and below. It routes all levels of hierarchy and is incremental, meaning that it does not change existing critical nets created by hand. When running the custom IC layout system, designers can select an area of the chip and have the integrated router route all of the nets within that window. Gateways that force a particular routing channel, as well as blockages, changes, and fixed and existing routes are all recognized by the router without data translation or having to save the data to disk.

With this interoperable solution in place, the design team is able to create layouts as before using the automated custom IC layout system with SDL methodology. Transistor-level routing is performed by the layout tool, as are the critical nets. Alternatively, pre-wires that define the routes

for critical nets can be defined by the layout editor. Routing is performed in phases, starting with critical nets and then proceeding in prioritized groups (hierarchically), or entire blocks can be done at once in just a few minutes.

The design team is also able to take advantage of the custom router's built-in extraction and timing engines for rapid feedback of parasitic interactions and simple timing. In this way, engineers can determine when the routing topology is "good enough" before committing too much to layout. Plus, the speed and controllability of this custom flow makes it feasible for them to quickly evaluate the placement of layout elements for optimal results. The router can also add 'dummy fill' (extra pieces of metal commonly inserted into layout to increase the data density for process uniformity and planarization) to help locate potentially destructive parasitic effects, thus ensuring that foundry-implemented dummy fill will not cause unexpected problems.

By combining these capabilities with a highly automated custom layout system, the design team, in collaboration with its EDA vendors, have created a solution that enables fast, iterative "what-if" analysis to simultaneously optimize the layout and routing. With the ability to iteratively route, extract, analyze timing, modify and verify, the design team can reduce the design margins required to achieve their higher performance

targets, while also reducing power consumption and area—all within less time than it previously took to implement a single layout.

Benchmarked results

The chosen benchmark involved a critical, high-performance block that had previously taken six weeks to converge on an acceptable solution. The performance requirements of this block conflicted with the area and power requirements which made it very difficult to complete successfully. To confirm the performance of the router, the existing routing was removed. The design was opened in the layout editor and the entire block was routed automatically within minutes. To mimic the standard flow, additional versions were quickly generated in which some of the critical nets were routed by hand using the layout editor and the remaining nets implemented using the automatic router. No critical nets were altered during the automated routing sequence and no DRC violations were noted.

After this initial proof of concept, the design team has demonstrated with consistent results that large, high-performance custom digital blocks, which typically took three to six weeks to complete, can be created in less than one week with their flow. This means the team can spend more time optimizing the performance, area and power consumption of custom blocks to ultimately deliver even greater value with their products.