synopsys®

DATASHEET

VC SpyGlass Fault Analysis

Fast Static Analysis to Guide Functional Safety and Reliability

Calculating ISO 26262 functional safety and reliability metrics to identify and address hotspots early in the design cycle and guide impactful design changes

Overview

Synopsys VC SpyGlass Fault Analysis performs functional safety and reliability analysis early in the design flow to provide guidance for design changes resulting in improved ISO 26262 functional safety or reliability metrics respectively. Leveraging SpyGlass technology, analysis can be performed either in RTL or gate-level netlists, minimizing impact to design schedules. Either transient faults or permanent faults can cause catastrophic failures during the operation of a safety-critical electronic device. The probability that an error can propagate to a safety-related signal is measured by the Single Point Fault Metric (SPFM) defined by the ISO 26262 functional safety standard. Minimum required SPFM values are documented by the standard for each of the defined automotive safety levels. VC SpyGlass Fault Analysis uses a static analysis approach (Figure 1), to accurately estimate the SPFM for any portion of a design.

Key Benefits

- Fast analysis at the RTL or gate-level ensures minimum impact to design schedule
- No testbenches required

Key Features

- Calculates the SPFM as specified in the ISO 26262 standard
- Reports with an ordered list of registers that can be replaced to improve SPFM metrics
- Intuitive, integrated browser with cross-probing among views

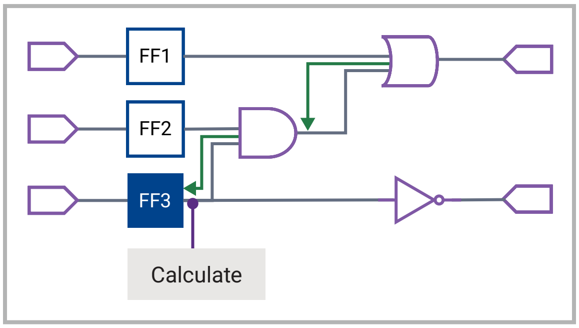

Figure 1: Static analysis approach to calculate single point fault metric

Static Calculation of Error Propagation

VC SpyGlass Fault Analysis uses static analysis to estimate the probability that an error can reach a safety-related signal. It calculates controllability and observability of logic signals in functional mode and supports multi-time-frame analysis with user-defined parameters to control the number of propagation levels. The calculation is done with respect to any user-specified safety related registers and outputs and can be performed on any portion of the design including top level. This provides the ability to identify and efficiently address SPFM hotspots. At the lowest level, a list of the design's flip-flops is generated and ordered based on each flop's contribution to SPFM loss (Figure 2). This makes it easier to determine the minimum number of regular flops that need to be replaced with error-tolerant flops to achieve the desired SPFM value. Flop substitutions are then performed within the synthesis and placeand-route flow based on the generated minimum list. Alternatively, larger blocks of logic contributing as a whole to SPFM loss can be managed using other techniques, such as adding redundant blocks or through the addition of safety monitors.

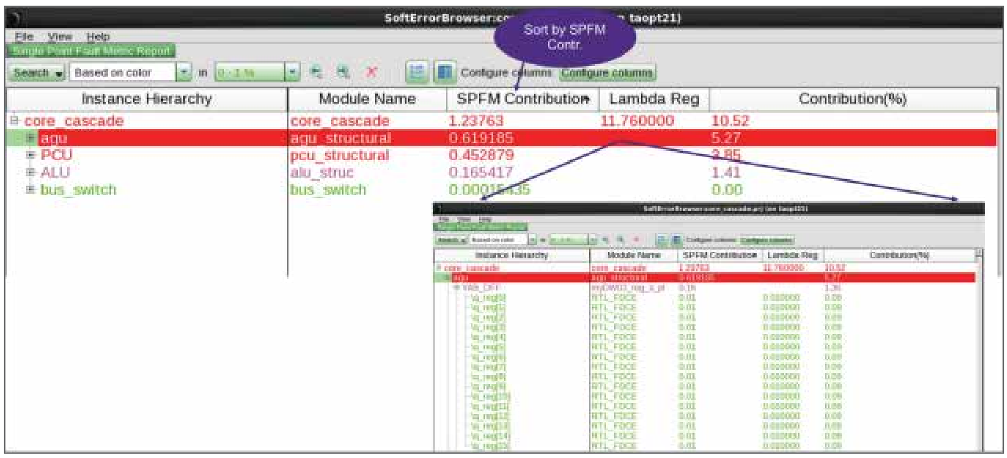

Figure 2: SPFM Browser identifies the blocks in the design with the highest probability causing functional safety failure

Key Features

VC SpyGlass Fault Analysis supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Verification: VCD, FSDBCalculates the SPFM as specified in the ISO 26262 standard

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com, contact your local sales representative or call 650.584.5000